

High-Speed Memory Access

by

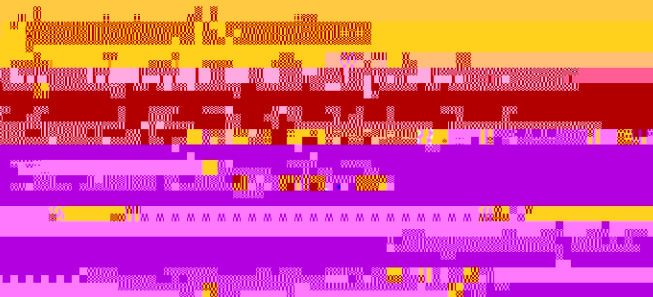
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Modern memory access technologies especially prefer a wide bus level.

As the farthest bank of storage voltage drop across the SRAM bus and the single bank the proposed RAMs in multiple physically separated locations.

Figure 1: Memory access diagram showing a bus structure with multiple banks.

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The diagram illustrates a memory access system with multiple physically separated banks. The bus structure is designed to minimize voltage drop across the SRAM bus, ensuring high-speed memory access. The control logic at the top manages the data flow between the banks and the bus.